

The Growing Impact of Atmospheric Radiation

Effects on Semiconductor Devices and the

Associated Impact on Avionics Suppliers

Introduction

There is a great need to increase the focus and attention of Avionics suppliers on the effects of atmospheric radiation on semiconductor devices. The continuing advancement of semiconductor technology is causing significant increases in Single Event Upset (SEU) susceptibility in semiconductor devices with the failure rate increasing exponentially. Contributing factors to the increase in failure rates include device geometry, voltages, cell density, etc. These factors are additive. While the changes and advancements by themselves exponentially impact SEU susceptibility they have also opened the door to the effects of thermal neutrons (slow neutrons). The effects of thermal neutrons have not previously been considered when evaluating SEU rates.

In the past, fast neutrons (high energy neutrons) were the main focus of SEU analysis in avionic equipment design. Part analysis was always done using high energy neutrons. Thermal neutrons seldom entered any discussion. The low energy level of thermal neutrons and their by-products were not thought to have significant effect on semiconductor devices. An international standard being developed by the International Electrotechnical Committee, (IEC) currently designated ¹IEC TS 62396-Part 1 addresses concerns about thermal neutrons in its Annex A - Thermal Neutron Assessment. This assessment proposes that thermal neutrons have the potential to be a bigger problem than fast neutrons.

Recent research has confirmed the importance of thermal neutron affects in SEU analysis. Not all integrated circuits are sensitive to thermal neutrons, but if they are sensitive the impact is usually significant. The controlling factor is the process used in making the particular integrated circuit (IC). Large IC vendors are adapting their fabrication processes to eliminate this thermal neutron sensitivity, but it will be years before they will accomplish this task.

This exponential rate of technology change has caused a dramatic and rapid shift in system level SEU rates. The result is some systems will not be capable of performing as designed in all operational environments. This performance impact is the result of using fault tolerant system design methodologies developed years ago to deal with a specific range of issues that existed at that time. The range of issues previously considered when validating system architectures have changed without the designer's awareness. This is resulting in potentially defective designs. The class of aircraft most vulnerable (for a

variety of contributing factors) is the military UAV's (Unmanned Aerial Vehicle). Unmanned Aerial Vehicles are being designed using large numbers of COTS (commercial off the shelf) equipment configured in classical redundant configurations. The redundant configurations may not support the reality of today's COTS components resulting in an unacceptably high probability of "loss of command and control". This exponential rate of technology change is occurring much faster than the feedback rate of field service data. The fast rate of technology change coupled with the slower rate of field feedback is resulting in many design groups and suppliers building equipment under design paradigms that are rapidly becoming invalid. In this information vacuum, the avionic industry is rapidly being exposed to considerable product liability risks with no idea that risk levels of this magnitude even exist.

Background of Atmospheric Radiation Effects on Semiconductors

A single event upset results from a single, energetic particle depositing a charge in a region of a semiconductor device causing it to change state or alter its analog output. The end result is an erroneous output from the device. The types of particles that contribute to this effect are alpha particles, various ions, protons, and neutrons. At sea level, the largest contributors are alpha particles (from packaging and lead), and neutrons. The exposure to all particle types increases as the latitude and altitude increases, especially during solar events.

Single event phenomena can be classified as three basic effects (in order of permanency):

1. (SEU) Single event upset (soft error)
2. (SEL) Single event latchup (soft or hard error)
3. (SEB) Single event burnout (hard failure)

Single event upset (SEU) is a condition that causes corruption of data or logic state in a device resulting in erroneous output. This is a soft error, meaning that data could be updated or corrected or the part reset and normal functionality would be resumed. This was first observed in 1975.

Single event latchup (SEL) is a condition in some CMOS devices where the energy deposited locally in a device by the single particle has turned on parasitic transistors causing high power supply current through the device. SEL also causes loss of device functionality. This can be a persistent failure and can only be cured by cycling power. This was first observed in 1979.

Single event burnout (SEB) is a condition in a high voltage device resulting from the energy deposition by a single particle leading to a feedback mechanism that exceeds the breakdown voltage and therefore destroys the device. SEB of power MOSFETs was first reported in 1986. Single Event Effects can also cause secondary breakdown in bipolar junction transistors (BJTs), resulting in burnout of the transistor as was first reported by Titus *et al.* in 1991.

The possibility of single-event upsets was first postulated by Wallmark and Marcus in 1962. The first actual satellite anomalies were reported by Binder *et al.* in 1975. Some of the early pioneering work was by May and Woods, who investigated alpha particle induced soft errors. In their work the source of alpha particles was not from space but rather from the natural decay of trace (ppm) concentrations of uranium and thorium present in integrated circuit packaging materials.

Nearly all semiconductor devices have been found to have some susceptibility to radiation effects in space and/or on earth. Up until recently, the effects have been detectable and very manageable due to the fact that they did not occur often enough in most environments to cause serious problems. This is largely due to simple physics. Single particles can only carry or induce a limited charge. Previous device geometries and operating voltages resulted in higher critical charge thresholds than most particles could deliver.

An additional factor is the variances in the radiation that cause SEUs. Solar affects can have a significant impact on radiation levels and resultant SEU rates. The sun on an eleven year cycle produces varying sizes of solar flares. These flares send out energetic particles that strike the earth and can affect the entire planet, but especially in the Polar Regions where the earth's magnetic field is weakest. These particles can cause an increase in the radiation that an aircraft sees by a factor ranging from 10-1000X. The next projected solar peak where these levels could occur is 2011. This change in radiation can equally impact SEU rates. For various reasons, this modifier has never been considered in SEU analysis.

Current State of SEU Issues

As has been stated, many integrated circuits, both analog and digital have been proven to have some susceptibility to atmospheric radiation effects. Knowledge of these issues has allowed system and circuit designers to modify system and board level designs to mitigate SEU effects. For analog devices, mitigation may take the form of enhanced part de-rating or signal filtering. For memory devices, error detection and correction are typically used. To validate these designs, device susceptibility testing is done to determine if a part is appropriate for use.

Design Processes are in place but architectural details are based on old paradigms.

SEU error rates used in system safety calculations are often derived from accelerated tests on semiconductor devices at facilities such as the Weapons Neutron Research Center (WNR) at Los Alamos National Labs. These accelerated rates derived from testing are normalized to standard atmospheric rates in the form of errors per hour for use in system safety calculations. In avionics design, the use of worst case analysis is a very common theme. The aircraft is expected to function in many thermal environments from desert to arctic. In like manner there is the same implied expectation that the aircraft should be able to fly regardless of geographic region or solar activity. Solar activity affects the entire planet on an eleven year cycle and the impact of these affects is significant and needs to be addressed in SEU analysis as a worst case condition. In years past, this worst case methodology was never applied to SEU rates, because doing so resulted in what would be considered analytical noise. After all these years the same practices have continued and there are no known companies using worst case analysis as applied to SEU's. This is not surprising since Boeing, Airbus and the military have no requirements driving this aspect of the issue.

If worst case analysis were applied rates would shift 50-100X.

In recent years, thermal neutrons have been discussed in research papers, but they have been largely ignored because of their low energy level. However, research and theoretical analysis has found that within an airframe at cruise altitudes, the thermal neutron density is equal to or greater than that of the atmospheric neutrons that exist outside the aircraft at that altitude. This is due to the collisions of the high energy neutrons with hydrogen atoms contained in fuel, baggage, passengers, etc. As was stated earlier, this has a significant impact on overall SEU rate, but from a safety analysis process viewpoint is still not considered in the scheme of things.

Thermal neutrons are not considered in analysis and as such will shift rates 2+X.

Many designers are aware of SEU issues, but it has not been considered a significant design factor. The military has no SEU requirements in terrestrial environments. Boeing and Airbus levy some basic SEU requirements but they do not begin to address the scope of the problem. For worst case analysis, neither Boeing, Airbus or the military have requirements driving this aspect of the issue. To address this gap, the International Electrotechnical Commission (IEC) has begun formulating a SEU standards document for the purpose of formalizing SEU analysis in Avionics systems design.

It is likely in several years that the FAA will formalize these aspects for certification.

For many years, atmospheric radiation has been a design concern but it has generally remained in the background and not of noteworthy practical design concern. For instance, if you have a box first delivered in 2001 with an MTBF (Mean Time Between Failures) of 50,000 hours and you have a box level SEU rate of 40,000 hours, who really cares? Applying worst case analysis here brings you down to an SEU rate of 1 soft failure per 400 hours, which still may not disturb anyone. The concern level is not very high and this is based on solid experience on products fielded just a few years ago. However, device SEU rates have shifted dramatically over the past few years. In 2005 an analysis of several "state of the art" COTS processing modules, which were advertised as being used in current military aircraft designs, revealed normalized module level SEU rates of 350 hours. This is only for those SEU faults that require a power cycle to correct.

This analysis did not take into account solar events or thermal neutron influence. Taking into account a moderate worst case solar modifier drops that rate down to less than 4 hours. Using average flight lengths results in an unacceptably high probability that all of this equipment would cease to function on a flight during a moderate solar event.

This is the collision of present reality against the perception of past engineering experience.

What Factors Are Driving This?

Key factors contributing to the current situation are:

1. Semiconductor design and use factors:
 - Lower operating voltage, linearly increases sensitivity to atmospheric radiation effects.
 - Shrinking geometries increase susceptibility by the square of the inverse. Moving from a .8 micron to .2 micron geometry increases susceptibility by 16X.
 - Failure rates are typically measured on a per bit basis. For higher complexity devices, consisting of more bits or gates, this translates into a greater probability for device errors.
 - When geometries reached $< .3$ um, additional fault modes became possible, which only magnifies and accelerates the problem.
2. Avionic design cycles that take 2-4 years from product concept to use of the product, combined with another 1-3 years before sufficient units are in service, mean that it can be several years before Suppliers start to see evidence from field service of issues related to susceptibility to atmospheric radiation effects.
3. Tight product design schedules and budgets may tend to limit design scrutiny.
4. Lack of research information on the effects of thermal neutrons.
5. Rapid rate of technology advancement makes it difficult for the average engineer to keep up with the issues associated with atmospheric radiation effects.
6. Solar events occur on 11 year cycles. They are a major contributor to the SEU rates and the next peak is in 2011. This current cycle began its decline just when technology crossed a sensitivity threshold resulting in a time of least probability of solar effect, which contributes to masking the problem.
7. Methods used to calculate the effects of atmospheric radiation on system reliability or availability are no longer adequate and have the potential of being in error by several orders of magnitude.

Some charts are included to pictorially describe the evolution of integrated circuits. Figure 1 shows the exponential growth in processor performance over the past 20 years.

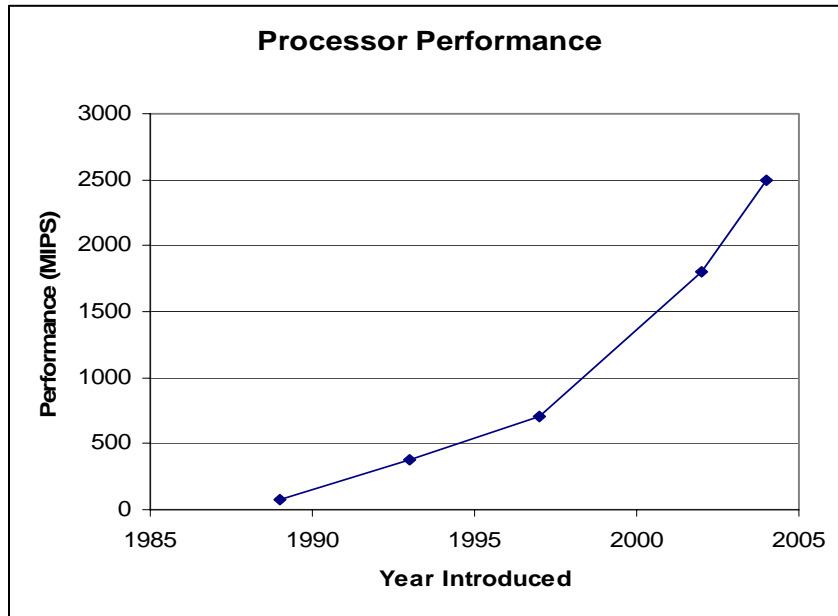


Figure 1 Processor Performance

Figure 2 shows a very steep acceleration in the density of processor designs to achieve the performance increases shown in Figure 1. SEU rates are usually measured in rate per bit. With the number of bits exponentially increasing, this results in an equivalent exponential increase in SEU for the processor as a component.

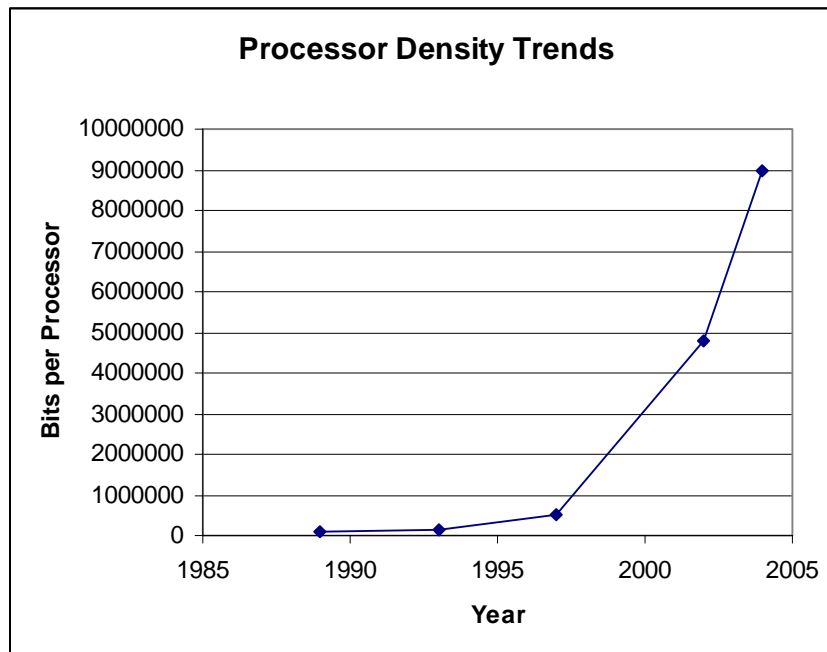


Figure 2 Processor Density Trends

The top line of Figure 3 shows the “nominal” potential for a processor to experience an SEU. The flatter middle line represents the hard failure rate based on an operational profile that includes worst case temperature conditions. As can be seen, pre 1990 the hard failure rate was the dominant component. Up to 1995, the event rates are almost equivalent. This history begins to explain why it has not caught the attention of design engineers.

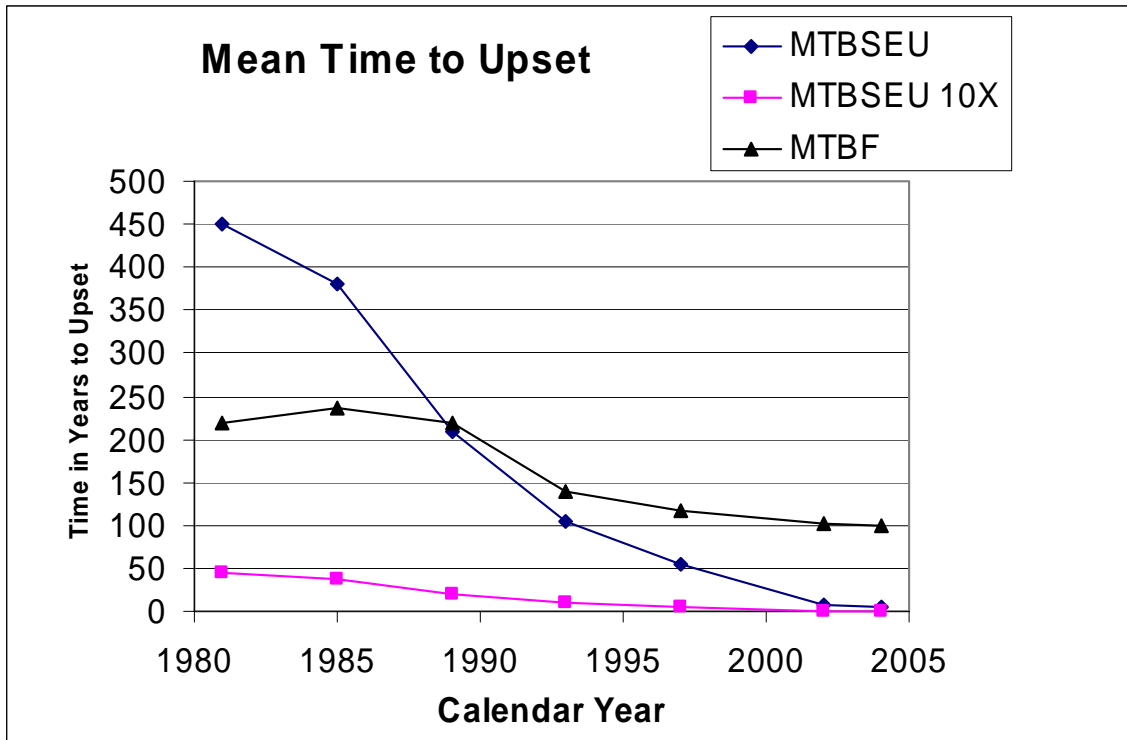


Figure 3 Mean Time to Upset

The bottom line in Figure 3 is a gentle attempt to describe a worst case. An aspect of every essential aircraft system design is the use of worst case analysis. Whether it is hot or cold; good weather or bad, every system is expected to continue functioning in any environment that the aircraft is permitted to occupy. However, in performing reliability and availability calculations, nominal or “normal” operating conditions are the only ones applied (the top line). Since SEU rates were less dominate than MTBF rates in the past, this worked well in describing system function. The bottom line on the graph represents a 10X worst case multiplier. This multiplier was chosen since a more appropriate multiplier of 100X would cause the bottom line to disappear into the lower axis.

This line represents an “optimistic” worst case rate. Current technology has reached a point where worst case must be considered and in these conditions, SEU rates can be measured in minutes or hours for many devices. Not taking this into account will result in designs that will not function in all of the environments intended.

Added to these impacts is the additional influence of thermal neutrons. In the past, a combination of larger device geometries coupled with higher operating voltages simply meant that it took a larger deposited charge to cause an SEU. As geometries have shrunk and voltages dropped, the deposited charge required to cause an SEU has dropped significantly. This increased sensitivity has opened the door to a much larger influence by thermal neutrons. Thermal neutrons themselves are typically < 1 eV (electron Volt), but their collision by-products are in the 1-2 MeV (Million Electron Volts) range, which is sufficient to cause upsets in the current technologies. Tests performed since 2000 in thermal neutron beams have verified this threat.

Industry as a whole has tended to treat atmospheric effects on semiconductors as status quo. Most engineers and managers are experiential people, meaning they make judgments and decisions based on previous experience or data. This is not a radical concept. However technological change has been exponential exceeding the previous rate of experiential feed back that engineers rely on and as a result, engineers simply have not kept up with the trend in atmospheric radiation susceptibility. In addition, thermal neutrons have never really been examined in depth. As we approach design regions where they have influence, little attention is being given.

Conclusion

This is not a mystical problem, but simply an information and technology application gap that has developed over time. The rate of change in the area of Single Event Upsets has been exponential and has resulted in a situation where the reality of SEU risks exceeds the attention, knowledge and priority of the companies building Avionics today. As a result, products are being designed and incorporated into military and commercial aircraft where the ability of these products to perform as advertised is in serious question. For avionics suppliers, this has the potential to create an intolerable liability and field support issue. For the commercial and military end users, this can translate into types of aircraft that would operate with limited mission capabilities or flight restrictions in certain geographic locations and grounding during significant solar events.

This issue has essentially crept up on the avionics industry as a whole. Just a few years ago, a design engineer would likely have considered using parts that would have experienced an SEU in 10 – 20 years based on nominal calculations. Today we are considering using parts on military and commercial aircraft designs that could have SEU rates measured in hours or days depending on worst case flight environments. For instance, using today’s parts could translate into a 10-20% processor failure rate during a single flight on an aircraft in northern latitudes during a moderate solar event. In analyzing some commercially available processor boards advertised as being used in existing military applications, combined board level SEU failure rates as calculated

during a moderate solar event are better measured in minutes or hours. Current design schemes and architectures are not robust enough to handle this failure rate. This needs to be addressed, because the best case scenario of staying on the current engineering design path will result in certification problems and likely flight restrictions in particular geographic regions. Those kinds of issues by themselves are extremely costly to any company that stumbles into these grounds. The risks are very high and action in the form of increased design scrutiny, development and analysis of more robust architectures, application of more stringent SEU related requirements and increased testing and sharing of SEU data between companies, etc. needs to be taken to mitigate these risks.

¹ IEC Technical Standard, IEC TS 62396 Part 1 “Process management for avionics - Accommodation of atmospheric radiation effects via single event effects within avionics electronic equipment,” March, 2006